(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
28 June 2001 (28.06.2001)

PCT

(10) International Publication Number
WO 01/47021 A1

(51) International Patent Classification[7]: H01L 27/146, H04N 3/15

(21) International Application Number: PCT/US00/32047

(22) International Filing Date:
21 November 2000 (21.11.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/468,696 21 December 1999 (21.12.1999) US

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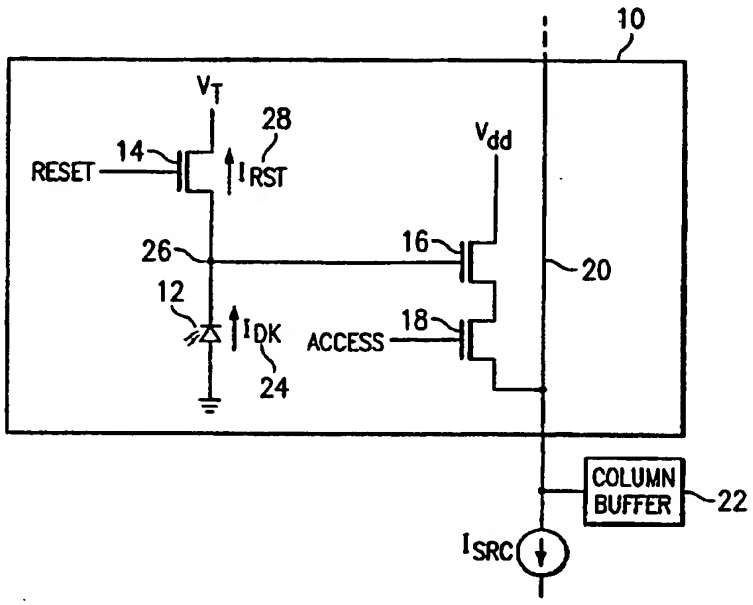
(81) Designated State *(national)*: JP.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— *With international search report.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD AND APPARATUS FOR ACHIEVING UNIFORM LOW DARK CURRENT WITH CMOS PHOTODIODES



(57) Abstract: An apparatus and method for achieving uniform low dark currents with CMOS photodiodes. A threshold voltage of reset FET is set to an appropriate value such that the dark current from a photodiode is actively removed through the reset FET during signal integration. This reduces the dark current by over 3 orders of magnitude as compared to conventional active pixel sensors, without requiring pinned photodiodes.

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DETAILED DESCRIPTION OF THE INVENTION

The following description is provided to enable any person skilled in the art to make and use the invention and sets forth the best modes contemplated by the inventor for carrying out the invention. Various modifications, however, will remain readily apparent to those skilled in the art, since the basic principles of the present invention have been defined herein specifically to provide an apparatus and method for achieving uniform low dark current with CMOS photodiodes.

Figure 1 illustrates a three-transistor active pixel sensor 10 that can advantageously apply the teachings of the present invention. In the preferred embodiment, each pixel 10 comprises a photodetector, such as a photodiode 12, which connects to a reset FET 14 and to a source follower amplifier FET 16. An access FET 18 connects the pixel output to a bus line 20, which in turn connects to a column buffer 22. The bus line 20 connects all the pixel outputs in a column of a photodetector array to the column buffer. A CMOS imager may be formed by a plurality of active pixel sensors 10 arranged in rows and columns to produce a two-dimensional array.

The photodiode 12 may comprise a substrate diode, for example, with the silicide cleared. In such an embodiment, which is preferred for compatibility with most CMOS processes, it is necessary to clear the silicide because it is opaque to visible light. Those skilled in the art will appreciate that the pixel 10 is preferably designed in the simplest form to obtain the largest available light detecting area while providing broad spectral response, and compatibility with standard CMOS production processes.

For maximum compatibility with standard submicron CMOS processes the photodiode 12 may be formed at the same time as the lightly doped drain (LDD) implant of n-type MOSFETs for the chosen process; this creates n-on-p photodiode junction in the p-type

FIG. 1

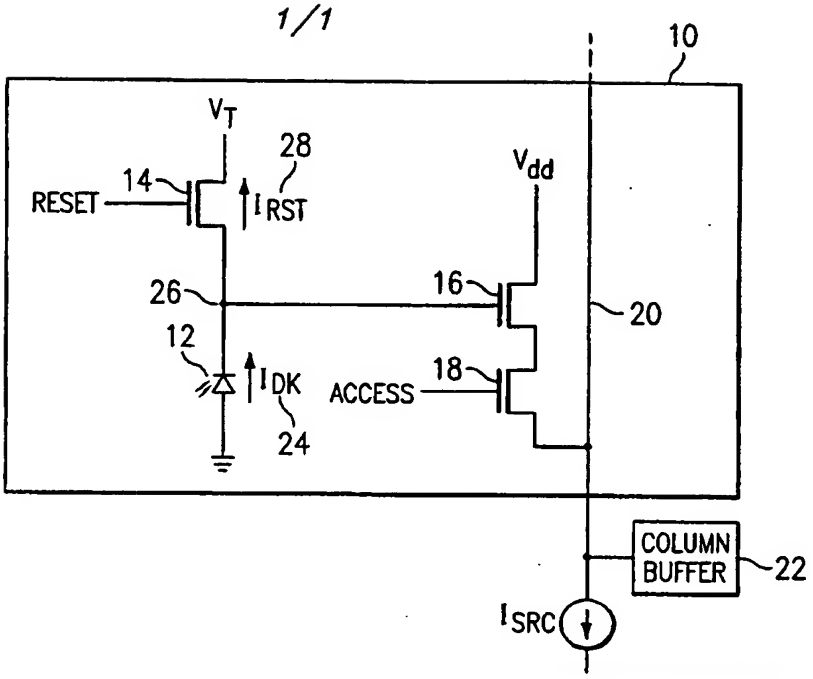
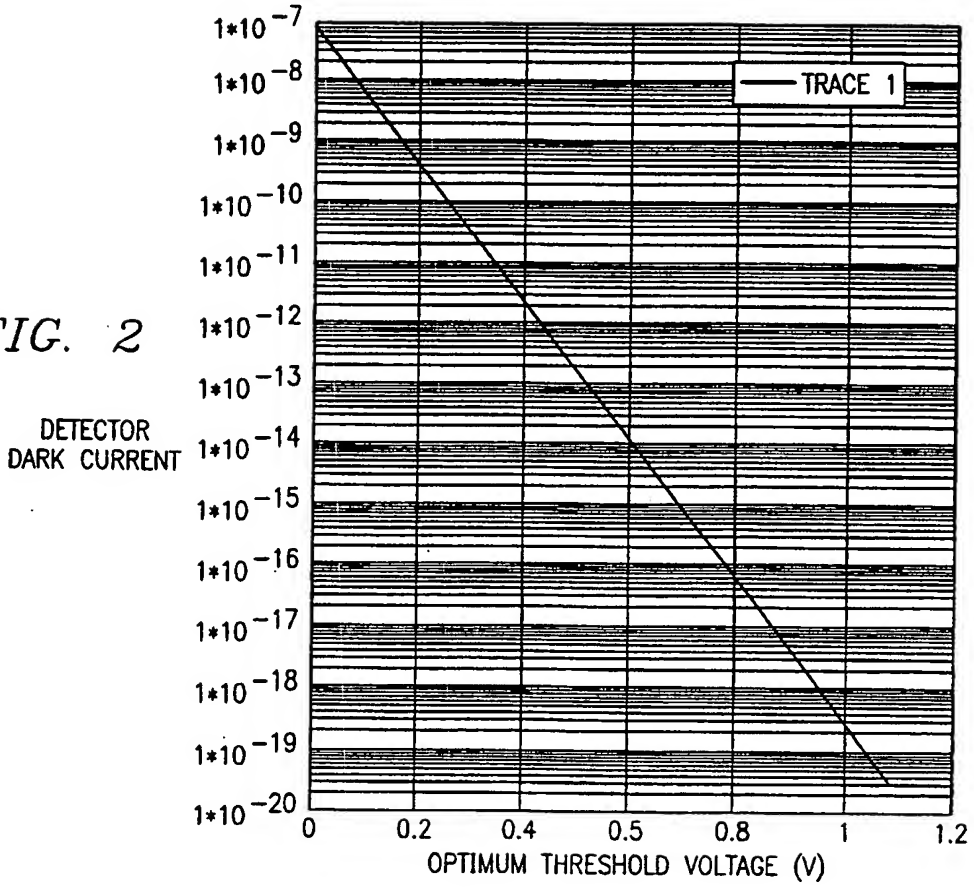

10
V_T
28
RESET
14
I_{RST}
V_{dd}
26
16
20
12
I_{DK}
ACCESS
18
24
COLUMN BUFFER
22
I_{SRC}

FIG. 2


DETECTOR DARK CURRENT
1*10⁻⁷
1*10⁻⁸
1*10⁻⁹
1*10⁻¹⁰
1*10⁻¹¹
1*10⁻¹²
1*10⁻¹³
1*10⁻¹⁴
1*10⁻¹⁵
1*10⁻¹⁶
1*10⁻¹⁷
1*10⁻¹⁸
1*10⁻¹⁹
1*10⁻²⁰
TRACE 1
0
0.2
0.4
0.5
0.8
1
1.2
OPTIMUM THRESHOLD VOLTAGE (V)